PATENT APPLICATION
DOCKET NO.: 200208009-1

REMARKS

Claims 1-20 are currently pending. Claims 1, 9, and 15 are in independent form.

Claims 1, 3-5, 7-10 and 15-16 have been amended by way of the present response. Support for the amendments can be found in the application, for example, in paragraphs [0028] and [0039], *inter alia*. No new matter is added hereby.

Favorable reconsideration of the present application as currently constituted is respectfully requested.

Regarding the Claim Rejections - 35 U.S.C. §102

In the pending Office Action, claims 1-14 are rejected under 35 U.S.C. §102(b) as being unpatentable over U.S. Patent Application 2001/0033630 to Hassoun *et al.* (hereinafter the *Hassoun* reference).

In connection with these rejections, the Examiner has commented as follows with respect to the *Hassoun* reference:

> 1) Regarding claim 1:
> Hassoun et al. discloses a system for compensating for skew in a programmable clock synchronizer for effectuating data transfer between first circuitry disposed in a first clock domain and second circuitry disposed in a second clock domain, wherein said first clock domain is operable with a first clock signal and

said second clock domain is operable with a second clock signal, said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, where N/M ≥ 1, comprising:

a phase detector operable to detect a phase between said first clock signal and said second clock signal (Paragraph 30 Line 5);

a skew state detector disposed in communication with said phase detector for generating a skew state signal which tracks a phase relationship between said first clock signal and said second clock signal (Paragraph 37 Lines 1-14, wherein, the decremented/incremented output signal of the counter is interpreted as the skew state signal) ...

9) Regarding claim 9:

Hassoun et al. teaches a method for compensating for skew in a programmable clock synchronizer for effectuating data transfer between first circuitry disposed in a first clock domain and second circuitry disposed in a second clock domain, wherein said first clock domain is operable with a first clock signal and said second clock domain is operable with a second clock signal, said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, where N ≥ M 1, comprising:

... determining if a state transition is necessary based on tracking the position of said coincident edges of said first and second clock signals (Paragraph 11 Lines 5-11 and Paragraph 37 Lines 7-14, wherein, 'determine whether to increase or decrease propagation delay', i.e., decrement/increment counter, is interpreted as determining if a state transition is necessary); and

generating a control signal indicative of said state transition, thereby compensating for said skew between said first clock signal and said second clock signal (Paragraph 37 Lines 7-14, wherein, decrement/increment output of the counter is interpreted as the control signal).

Applicant respectfully submits that the pending §102(b) rejections as set forth above have been overcome or otherwise rendered moot by way of the present amendment. An embodiment as defined by base claim 1 is directed to a system for compensating for skew in a programmable clock synchronizer for effectuating data transfer between first circuitry in a first clock domain and second circuitry in a second clock domain, the two clock domains having respective first and second clock signal that have a ratio of N first clock cycles to M second clock cycles, where $N/M \geq 1$. As currently constituted, the embodiment of base claim 1 involves, *inter alia*, a skew state detector that generates a skew state signal which tracks the phase relationship between the two clock signals relative to the zero point of a timing window corresponding to said second clock signal.

Base claim 9 is directed to a method for compensating for skew in a programmable clock synchronizer for effectuating data transfer between first circuitry disposed in a first clock domain and second circuitry disposed in a second clock domain, the first and second clock domains having respectively first and second clock signals that have a ratio of N first clock cycles to M second clock cycles, where $N/M \geq 1$. As currently constituted,

the embodiment of base claim 9 involves, *inter alia*, determining the phase difference between the first clock signal and the second clock signal relative to a zero point of a timing window corresponding to the second clock signal.

In both of these base claims, the relationship between the two clock signals is determined relative to a zero point of the timing window of one of the signals.

The *Hassoun* reference is directed to using a clock phase shifter with a delay line to synchronize a reference clock signal with a skewed clock signal. See Abstract.

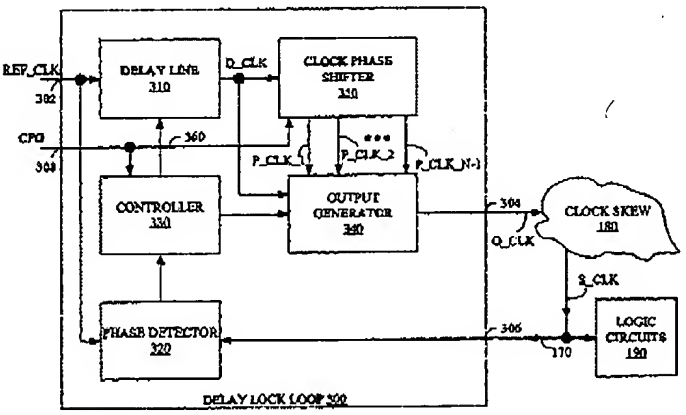

FIGURE 3

As disclosed with reference to Figure 3 of *Hassoun*, excerpted herein for convenience, delay lock loop 300 contains a delay line 310, a clock phase shifter 350, a controller 330, an output generator 340, and a phase detector 320. Among other actions, phase detector 320 informs controller 330 whether the propagation delay D from delay line 310 should be increased or decreased to

achieve synchronization of skewed clock signal S_CLK with reference clock signal REF_CLK. For some embodiments of phase detector 320, a jitter filter (not shown) can be used to reduce clock jitter. *Hassoun* further describes that in one embodiment, the jitter filter is an up/down counter (not shown) that decrements by one if the propagation delay should be decreased and increments by one if propagation delay should be increased. Although the Examiner appears to read the up/down counter on the skew state signal in the current Office Action, the up/down counter does not track the phase relationship between the first clock signal and the second clock signal relative to a zero point of a timing window corresponding to the second clock signal, as now recited in base claims 1 and 9. Additionally, it appears that the overall teachings of *Hassoun* fail to anticipate or suggest this feature.

For at least the foregoing reasons, pending base claims 1 and 9 are believed to be patentable over the *Hassoun* reference. Additionally, dependent claims 2-8 (depending from base claim 1) and dependent claims 10-14 (depending from base claim 9) are also believed to be in condition for allowance over the applied art for the same reasons.

Regarding the Claim Rejections - 35 U.S.C. §103

In the pending Office Action, claims 15-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over the *Hassoun* reference in view of U.S. Patent 6,182,236 to Culley *et al.* (hereinafter, the *Culley* reference).

In connection with these rejections, the Examiner has commented as follows with respect to the references, i.e., the *Hassoun* reference and the *Culley* reference, as applied against base claim 15:

> 1) Regarding claim 15:
> Hassoun et al. discloses:
> ... means for determining if a state transition is necessary based on tracking the position of said coincident edges of said first and second clock signals (Paragraph 11 Lines 5-11 and Paragraph 37 Lines 7-14, wherein, 'determine whether to increase or decrease propagation delay', i.e., decrement/increment counter, is interpreted as determining if a state transition is necessary); and
> means for generating a control signal indicative of said state transition, thereby compensating for said skew between said first clock signal and said second clock signal (Paragraph 37 Lines 7-14, wherein, decrement/increment output of the counter is interpreted as the control signal).
> Hassoun et al. does not disclose a computer system having an apparatus for compensating for skew in a programmable clock synchronizer for effectuating data transfer ... However, Culley et al. discloses a computer system having an apparatus for compensating

> for skew in a programmable clock synchronizer for effectuating data transfer between first circuitry disposed in a first clock domain and second circuitry disposed in a second clock domain, wherein said first clock domain is operable with a first clock signal and said second clock domain is operable with a second clock signal, said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, where $N/M \geq 1$ (Column 4 Lines 43-53).
>
> It is desirable to have a computer system with an apparatus for compensating for skew. This allows the clocking signal arriving at the various computer subsystems to be synchronized, and therefore, allow for accurate and proper communication of data within the computer system (See Culley et al., Column 4 Line 65 to Column 5 Line 8). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the computer system of Culley et al. include Hassoun et al.'s apparatus for compensating for skew, in order to allow the clocking signal arriving at the various computer subsystems to be synchronized, and therefore, allow for accurate and proper communication of data within the computer system.

Applicant respectfully submits that the pending §103(a) rejections as set forth above have been overcome or otherwise rendered moot by way of the present amendment. An embodiment as defined by base claim 15 is directed to a computer system having an apparatus for compensating for skew in a programmable clock synchronizer for effectuating data transfer between first circuitry disposed in a first clock domain and second circuitry disposed in a second clock domain, wherein the first clock domain

is operable with a first clock signal and the second clock domain is operable with a second clock signal, the first and second clock signals having a ratio of N first clock cycles to M second clock cycles, where N/M ≥ 1. As currently constituted, the embodiment of base claim 15 involves, *inter alia*, means for determining a phase difference between the first clock signal and the second clock signal relative to a zero point of a timing window corresponding to the second clock signal.

Hassoun is deficient when applied as a primary reference with respect to the claimed means for determining a phase difference between said first clock signal and said second clock signal relative to a zero point of a timing window corresponding to said second clock signal. On the other hand, reliance on the secondary reference, i.e., the *Culley* reference, is of no avail in this context either. The *Culley* reference is directed to a clock generation circuit to adjust the phase of a clocking signal provided to various subsystems of an electronic system. See Abstract. This reference does not make up for the deficiencies of *Hassoun*, nor does the Examiner suggest that *Culley* does so. Simply stated, *Culley* does not disclose any structure or functionality with respect to tracking the phase relationship

between the first clock signal and the second clock signal relative to a zero point of a timing window corresponding to the second clock signal.

Accordingly, for at least the foregoing reasons, base claim 15 is believed to be allowable over the combination of the *Hassoun* and *Culley* references. Likewise, dependent claims 16-20, which depend from base claim 15, are also in condition for allowance over *Hassoun* and *Culley*.

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SUMMARY AND CONCLUSION

In view of the fact that none of the art of the record, whether considered alone or in combination discloses, anticipates or suggests the pending claims, and in further view of the above remarks and/or amendments, reconsideration of the Action and allowance of the present patent application are respectfully requested and are believed to be appropriate.

Respectfully submitted,

Dated: 1/16/2007

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